Application # 09/758,573
Submitted June 15, 2004
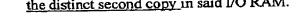Reply to Office Action of December 15, 2003

I.   LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1.   (amended) A method of increasing image processing performance by <u>explicitly copying a first instance of an image existing in an I/O RAM into an extra second copy of said image in a buffer in memory prior to performing CPU intensive operations on the data copied from said image, wherein the CPU access is made directly to the extra second copy of the data in memory and not to the first instance in said I/O RAM</u> image data between a memory and an I/O RAM.

2.   (original) The method of claim 1 wherein said memory is cached.

3.   (original) The method of claim 1 wherein said memory is cached in a CPU cache.

4.   (original) The method of claim 1 wherein said memory is cached in an external cache.

5.   (original) The method of claim 1 wherein said copying in accomplished by DMA circuitry.

6.   (original) The method of claim 1 wherein said copying in accomplished by calling a memory copy function.

7.   (original) The method of claim 6 wherein said image data is copied in a single call to said memory copy function.

8.   (original) The method of claim 6 wherein a subset of said image data is copied one line at a time by repeated calls to said memory copy function.

9.   (original) The method of claim 6 wherein a subset of said image data is copied by repeated calls to said memory copy function.

10.   (canceled)

11.   (amended) The method of claim 10 <u>claim 1</u> wherein said I/O RAM is associated with a video digitizer.

12.   (amended) The method of claim 1 wherein a buffer in said memory is copied to an image <u>A method of increasing image processing performance by explicitly storing the processed results of CPU intensive operations in a first instance of a buffer in memory prior to copying the processed data into a distinct second copy of the processed data in an image in an I/O RAM, wherein the CPU results are written directly to the first instance of the processed data in memory and not to the distinct second copy in said I/O RAM.</u>

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13. (original) The method of claim 12 wherein said I/O RAM is associated with a video output device.

14. (original) The method of claim 13 wherein said video output device drives a computer monitor.

15. (original) The method of claim 13 wherein said video output device outputs video signals.

16. (amended) A machine for image processing comprising:

    (a) a memory for storing an image;

    (b) a processor for processing said image;

    (c) an I/O device; and

    (d) a means for copying image data between said memory and said I/O device, wherein said image data is copied from said I/O device to a second copy of said image data in a buffer in said memory prior to being processed by said processor or wherein said processor processes said image data using a buffer in said memory before copying the processed image data from said memory to said I/O device,

whereby image processing time is reduced.

17. (original) The machine of claim 16 wherein said I/O device is a means for inputting an image.

18. (original) The machine of claim 16 wherein said I/O device is a means for outputting an image.

19. (original) The machine of claim 16 where said processor executes programs to enhance, compress, encrypt, or reformat said image data.

20. (original) The machine of claim 16 where said processor executes programs to decrypt, decompress, or enhance said image data.

21. (amended) A network of machines comprising:

    (a) one or more first machines which implement(s) the method of ~~claim 10~~ claim 1; and

    (b) one or more second machines which implement(s) the method of claim 12,

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whereby a video signal is digitized and encoded by at least one of said first

machines, transmitted across said network to other of said second machines that

decode and output the results.

22.   (new) A machine for image processing comprising:

(a)   an image input device having image data;

(b)   a processor for processing said image data, connected to said input device;

(c)   a memory, connected to said processor;

(d)   a means for copying said image data from said input device to a second copy of said image data in a buffer in said memory prior to being processed by said processor, whereby image processing time is reduced compared to the image processing time required if the processor processed the first copy of the image data in the input device.

23.   (new) The machine of claim 22 where said processor performs image processing to enhance or reformat said image data.

24.   (new) The machine of claim 22 where said processor performs image processing to encrypt said image data.

25.   (new) The machine of claim 22 where said processor performs image processing to compress said image data.

26.   (new) A machine for image processing comprising:

(a)   an image output device requiring image data for output;

(b)   a processor for generating said image data, connected to said output device;

(c)   a memory, connected to said processor;

(d)   a means for copying, after said processor generates a first set of image data in said memory, said first set of image data from said memory to a second copy of said image data in said output device, whereby image processing time is reduced compared to the image processing time required if the processor generated the image data directly in said input device instead of said memory.

27.   (new) The machine of claim 26 where said processor performs image processing to enhance said image data prior to copying to the output device.

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28. (new) The machine of claim 26 where said processor performs image processing to decrypt said image data prior to copying to the output device.

29. (new) The machine of claim 26 where said processor performs image processing to decompress said image data prior to copying to the output device.

30. (new) The method of claim 12 wherein said copying is accomplished by DMA circuitry.

31. (new) The method of claim 12 wherein said copying is accomplished by calling a memory copy function.

32. (new) The machine of claim 16 wherein said means for copying includes DMA circuitry.

33. (new) The machine of claim 22 wherein said means for copying includes DMA circuitry.

34. (new) The machine of claim 26 wherein means for copying includes DMA circuitry.